IN THE SPECIFICATION

Please amend the paragraph beginning at page 4, line 20 as follows:

The run-length ~~decoder~~ encoder, if enabled, encodes the run-length of the data it receives, in accordance with one of several modes. Bits associated with the run-length encoder in the configuration register select the mode in which the run-length encoder operates.

Please amend the paragraph beginning at page 5, line 20 as follows:

Fig. 1 shows the vector pipeline unit (VPU) 100, which is part of the video encoder/decoder that encodes/decodes video data, in accordance with one embodiment of the present invention. VPU 100 includes, among other components, run-length decoder 10, binary arithmetic logic unit (ALU) 12, binary multiplier/divider 14, accumulator ~~22~~ 18, barrel shifter ~~24~~ 20, round/modify logic unit ~~26~~ 22, saturate logic unit ~~28~~ 24, status register ~~30~~ 26, and run-length encoder ~~32~~ 28. It takes 1 clock cycle for each of the above components of VPU 100 to perform one of their respective operations.

Please amend the paragraph beginning at page 5, line 31 as follows:

The video encoder/decoder 150 (shown in Fig. 2)—in which VPU 100 of Fig. 1 is disposed—includes a 128-bit configuration register which includes register bits for enabling or disabling as well as controlling the operation of any one of the run-length decoder 10, ALU 12, binary multiplier/divider 14, accumulator ~~22~~ 18, barrel shifter ~~24~~ 20, round/modify logic unit ~~26~~ 22, saturate logic unit ~~28~~ 24, status register ~~30~~ 26, and run-length encoder ~~32~~ 28. Table 1 below includes a brief description of each bit of the configuration register. More detailed description of the relevant bits are described below.

IN THE CLAIMS

1. (Canceled)

2. (Currently Amended) The video encoder/decoder of Claim ~~1~~ 5, wherein the video encoder/decoder is configured by the processor a second time only if a second one of the plurality of data compression/decompression standards different from the first one of the plurality of data compression/decompression standards is selected for encoding/decoding.

3. (Original) The video encoder/decoder of Claim 2 wherein the video encoder/decoder is configured by configuring a configuration register disposed within the video encoder/decoder.

4. (Currently Amended) The video encoder/decoder of Claim 3 further comprising a memory which stores ~~the~~ configuration data for each of the plurality of data compression/decompression standards, wherein the processor reads the configuration data from the memory and loads the same into the configuration register.

5. (Currently Amended) ~~The video encoder/decoder of Claim 1 further comprising a vector pipeline unit, the vector pipeline unit further comprising:~~ A video encoder/decoder coupled to a processor, wherein the video encoder/decoder is configured by the processor a first time to encode/decode data in accordance with a first one of a plurality of data compression/decompression standards, and further including a vector pipeline unit comprising a run-length decoder which receives data elements of a data vector at its input terminals and decodes and supplies to its output terminals one of the data elements received thereby if the run-length decoder is disabled and a run-length of the data elements received thereby if the run-length decoder is enabled, wherein each data element comprises a plurality of bits.

6. (Original) The video encoder/decoder of Claim 5 wherein the run-length decoder is disabled if a bit associated therewith in the configuration register is reset.

7. (Currently Amended) The video encoder/decoder of Claim 6 wherein the vector

pipeline unit further comprises:

an ALU having a plurality of first input terminals which receive the data element supplied thereto by the run-length decoder, a plurality of second input terminals which receive a second data element of the vector and a plurality of output terminals~~,~~ the ALU to deliver to its output terminals one of a result of a plurality of arithmetic or logic operations performed thereby if the ALU is enabled and the first data element received at its first input terminals if the ALU is disabled.

8. (Original) The video encoder/decoder of Claim 7 wherein the ALU is disabled if a bit associated therewith in the configuration register is reset.

9. (Currently Amended) The video encoder/decoder of Claim ~~8~~ 7, wherein the vector pipeline unit further comprises:

a multiplier/divider having a plurality of first input terminals which receive the data supplied to the output terminals of the ALU, a plurality of second input terminals which receive a third data element of the vector, the multiplier/divider to supply to its output terminals a result of one of a plurality multiplication/division operations performed thereby if the multiplier/divider is enabled and the data received at its plurality of first input terminals if the multiplier/divider is disabled.

10. (Original) The video encoder/decoder of Claim 9 wherein the multiplier/divider is disabled if a bit associated therewith in the configuration register is reset.

11. (Currently Amended) The video encoder/decoder of Claim ~~10~~ 9, wherein the vector pipeline unit further comprises:

a multiplexer having a plurality of first input terminals which receive a fourth data element, a plurality of second input terminals which receive the data supplied to the output terminals of the multiplier/divider, a third input terminal and a plurality of output terminals, wherein the third input terminal selects and transfers to the multiplexer's output terminals one of the data supplied to the multiplexer by the multiplier/divider and the fourth data.

12. (Original) The video encoder/decoder of Claim 11 wherein the multiplexer transfers to its output terminals the data supplied thereto by the multiplier/divider if a bit associated with the multiplexer in the configuration register is reset.

13. (Currently Amended) The video encoder/decoder of Claim ~~12~~ 11, wherein the vector pipeline unit further comprises:

an accumulator having a plurality of first input terminals which receive the data supplied to the multiplexer's output terminals, and a plurality of second input terminals which receive the second data element of the vector, the accumulator to supply to its output terminals a result of one of a plurality of arithmetic operations performed thereby if the accumulator is enabled and the data received at its plurality of first input terminals if the accumulator is disabled.

14. (Original) The video encoder/decoder of Claim 13 wherein the accumulator is disabled if a bit associated therewith in the configuration register is reset.

15. (Currently Amended) The video encoder/decoder of Claim ~~14~~ 13, wherein the vector pipeline unit further comprises:

a barrel shifter having a plurality of first input terminals which receive the data supplied to the output terminals of the accumulator, wherein the barrel shifter right shifts the data it receives at its plurality of first input terminals if the barrel shifter is enabled.

16. (Currently Amended) The video encoder/decoder of Claim 15 wherein the barrel shifter supplies to its output terminals the data it receives at its plurality of first input terminals if the barrel shifter is disabled.

17. (Original) The video encoder/decoder of Claim 16 wherein the barrel shifter is disabled if a bit associated therewith in the configuration register is reset.

18. (Currently Amended) The video encoder/decoder of Claim ~~8~~ 15, wherein the vector pipeline unit further comprises a round logic unit which receives the data supplied thereto by the barrel shifter and rounds the received data to a nearest integer number, wherein the ~~vector~~

~~pipeline unit further comprises:~~

~~a~~ round logic unit ~~which~~ receives the data supplied thereto by the barrel shifter and rounds the received data to a nearest integer number if the round logic is enabled, wherein the round logic unit supplies the rounded data to its output terminals.

19. (Original) The video encoder/decoder of Claim 18, wherein the round logic unit delivers to its output terminals the data supplied thereto by the barrel shifter if the round logic unit is disabled.

20. (Original) The video encoder/decoder of Claim 19 wherein the round logic unit is disabled if a bit associated therewith in the configuration register is reset.

21. (Currently Amended) The video encoder/decoder of Claim ~~20~~ 18, wherein the vector pipeline unit further comprises:

a modify logic unit which receives the data supplied thereto by the round logic unit and modifies the received data to one of odd and even number if the modify logic unit is enabled, wherein the modify logic unit supplies the modified data to its output terminals.

22. (Original) The video encoder/decoder of Claim 21, wherein the modify logic unit delivers to its output terminals the data supplied thereto by the round logic unit if the modify logic unit is disabled.

23. (Original) The video encoder/decoder of Claim 22 wherein the modify logic unit is enabled or disabled by varying a bit associated therewith in the configuration register.

24. (Currently Amended) The video encoder/decoder of Claim ~~8~~ 21, wherein the vector pipeline unit further comprises:

a saturate logic unit which receives the data supplied thereto by the modify logic unit, the saturate logic unit to saturate the received data to a ~~saturate~~ saturation high value if the received data is greater than the ~~saturate~~ saturation high value and if the saturate logic unit is enabled, the saturate logic unit to saturate the received data to a ~~saturate~~ saturation low value if the received

data is smaller than the ~~saturate~~ saturation low value and if the saturate logic unit is enabled, wherein the saturate logic unit supplies to its output terminals the saturate data.

25. (Original) The video encoder/decoder of Claim 24 wherein the saturate logic unit supplies to its output terminals data it receives from the output terminals of the modify logic unit if the saturate logic unit is disabled.

26. (Original) The video encoder/decoder of Claim 25 wherein the saturate logic unit is enabled or disabled by varying a bit associated therewith in the configuration register.

27. (Currently Amended) The video encoder/decoder of Claim ~~26~~ 24, wherein the vector pipeline unit further comprises a status register which collects data supplied thereto by the saturate logic unit and supplies the collected data to ~~a~~ the processor, if the status register is enabled.

28. (Original) The video encoder/decoder of Claim 27 wherein the status register is enabled or disabled by varying a bit associated therewith in the configuration register.

29. (Currently Amended) The video encoder/decoder of Claim ~~8~~ 24, wherein the vector pipeline unit further comprises a run-length encoder which receives and encodes the run-length of the data that is supplied thereto by the saturate logic unit if the run-length encoder is enabled.

30. (Currently Amended) The video encoder/decoder of Claim ~~27~~ 29, wherein the run-length encoder is enabled or disabled by varying a bit associated therewith in the configuration register.

31-36. (Canceled)

Objection to the Disclosure

The disclosure is amended to correct various clerical errors.

Objection to Claims

Claims 5-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

In response thereto, Claim 5 is amended to include all of the limitations of base claim 1, and is therefore now allowable.

Claims 6-30 depend from Claim 5 and therefore distinguish over the cited references for at least the same reasons as Claim 5.

Rejection of Claims under 35 USC §112

Claims 18-30 are rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In response thereto, Claim 18 is amended to depend from Claim 15 to provide proper antecedent basis for the "barrel shifter," Claim 24 is amended to depend from Claim 21 to provide proper antecedent basis for the "modify logic unit," and Claim 29 is amended to depend from Claim 24 to provide proper antecedent basis for the "saturate logic unit."

Rejection of Claims under 35 USC §102

Claims 1-4 and 31-36 are rejected under 35 USC §102 as anticipated by U.S. Patent No. 5,926,208 to Noonen et al.

Claims 1 and 31-36 are canceled, and thus their rejection is now moot.

Claims 2-4 now depend from Claim 5, which as indicated above is allowable, and therefore Claims 2-4 distinguish over the cited references for at least the same reasons as Claim 5.

CONCLUSION

In light of the above remarks, it is believed that Claims 2-30 are in condition for allowance and, therefore, a Notice of Allowance of Claims 2-30 is respectfully requested. If the Examiner's next action is other than allowance as requested, the Examiner is requested to call the undersigned at (415) 291-9497.

Respectfully submitted,

Dated: September 13, 2004

William L Paradice III
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CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450 on September 13, 2004.

By: _____
William L Paradice III